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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,167	01/13/2004	Shunpei Yamazaki	0553-0393	3564

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Ek

Office Action Summary	Application No. 10/757,167	Applicant(s) YAMAZAKI ET AL.
	Examiner Christy L. Novacek	Art Unit 2822

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/21/04*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed January 14, 2004.

Specification

The disclosure is objected to because of the following informalities: At line 15 on page 15, "1D" should be replaced with "2D" in order to be in accordance with the drawings.

The abstract of the disclosure is objected to because "reduces" should be changed to "reduced" (last line). Correction is required. See MPEP § 608.01(b).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4, 8-12, 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 2 of claim 1 recites the limitation of "the substrate". There is insufficient antecedent basis for this limitation in the claim.

Line 2 of claim 4 and line 2 of claim 8 recite the limitation of "said semiconductor device". There is insufficient antecedent basis for this limitation in these claims.

Line 8 of claim 9 recites the limitation of "the semiconductor". However, line 1 of the claim recites "a semiconductor device" and line 3 of the claim recites "a semiconductor layer". Therefore, it is unclear as to which of these elements "the semiconductor" is referring.

Line 2 of claim 10 and line 2 of claim 14 recites the limitation of "the conductive layer". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 8, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sirringhaus et al. (US 20030059987) in view of Yudasaka et al. (US 6,514,801).

Regarding claim 1, Sirringhaus discloses forming a conductive layer (2/3/6) over a substrate (1) having an insulating surface by discharging a conductive material and performing a heat treatment over the conductive layer (para. 71-72). Sirringhaus does not disclose what type of heat mechanism is used to conduct the heat treatment step. Like Sirringhaus, Yudasaka discloses a method of forming the conductive wirings of a TFT by depositing a liquid conductive material on the surface of the substrate and then annealing the liquid material to evaporate the solvent therefrom. Yudasaka teaches that a heat lamp is an effective heat mechanism to evaporate the solvent from the liquid conductive material (col. 6, ln. 43-58). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a heat lamp to carry out the heat treatment step of Sirringhaus because Sirringhaus does not disclose any particular heating mechanism and Yudasaka teaches that a heat lamp can successfully evaporate the solvent from a liquid conductive mixture such as that of Sirringhaus.

Regarding claims 4, 8 and 12, Sirringhaus discloses that the conductive layer is formed within a semiconductor device that can be incorporated into a display device (para. 156).

Regarding claim 5, Sirringhaus discloses forming a conductive layer by discharging a conductive material so as to contact with source or drain wirings of a transistor and performing a heat treatment over the conductive layer (para. 71-72). Sirringhaus does not disclose what type of heat mechanism is used to conduct the heat treatment step. Like Sirringhaus, Yudasaka discloses a method of forming the conductive wirings of a TFT by depositing a liquid conductive material on the surface of the substrate and then annealing the liquid material to evaporate the solvent therefrom. Yudasaka teaches that a heat lamp is an effective heat mechanism to evaporate the solvent from the liquid conductive material (col. 6, ln. 43-58). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a heat lamp to carry out the heat treatment step of Sirringhaus because Sirringhaus does not disclose any particular heating mechanism and Yudasaka teaches that a heat lamp can successfully evaporate the solvent from a liquid conductive mixture such as that of Sirringhaus.

Regarding claim 9, Sirringhaus discloses laminating a semiconductor layer (4) and a gate insulating layer (5) over a substrate (1) having an insulating surface, forming a gate electrode (6) over the gate insulating layer by discharging a conductive material, forming an insulator layer (42) over the gate electrode and forming a contact hole for exposing the semiconductor layer to the insulating layer, forming source or drain wirings by discharging conductive material so as to fill the contact hole, and performing a heat treatment over the gate electrode and the source/drain wirings (para. 152, 158-159). Sirringhaus does not disclose what type of heat mechanism is used to conduct the heat treatment step. Like Sirringhaus, Yudasaka discloses a method of forming

the conductive wirings of a TFT by depositing a liquid conductive material on the surface of the substrate and then annealing the liquid material to evaporate the solvent therefrom. Yudasaka teaches that a heat lamp is an effective heat mechanism to evaporate the solvent from the liquid conductive material (col. 6, ln. 43-58). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a heat lamp to carry out the heat treatment step of Sirringhaus because Sirringhaus does not disclose any particular heating mechanism and Yudasaka teaches that a heat lamp can successfully evaporate the solvent from a liquid conductive mixture such as that of Sirringhaus.

Claims 2, 3, 6, 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sirringhaus et al. (US 20030059987) in view of Yudasaka et al. (US 6,514,801) as applied to claims 1, 5 and 9 above, and further in view of Speakman (US 6,713,389).

Regarding claims 2, 3, 6, 7, 10 and 11, Sirringhaus does not disclose the pressure at which the conductive layer is formed. Like Sirringhaus, Speakman discloses a method of forming conductive wirings of a semiconductor device by depositing droplets of a liquid conductive mixture on the surface of the substrate. Speakman teaches that it is advantageous to form the conductive droplets in a reduced pressure atmosphere because in higher pressures, the droplets will become deformed which impairs its dimensional stability and placement accuracy (col. 40, ln. 10-14). Speakman states that the reduced pressure atmosphere can be in the range of 1×10^5 to 1×10^{-6} N/m^2 (Pa) (col. 4, ln. 6-28).

Claims 13, 16, 17, 20, 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (US 6,362,507) in view of Jacobson et al. (US 6,294,401).

Regarding claim 13, Ogawa discloses forming a gate electrode (202-204) over a substrate (201) having an insulating surface, laminating a semiconductor layer (209), a channel protection layer (219-222), and a semiconductor layer (214-218/223-230/233-234/239-240) having one of n-type or p-type conductivity over the gate electrode, and forming source or drain wirings (243-247) over the semiconductor layer having the n-type or p-type conductivity (col. 9, ln. 11 – col. 11, ln. 67). Ogawa discloses that the gate electrode and the source/drain wirings are formed by sputtering instead of by discharging conductive material. Like Ogawa, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the gate electrode and the source/drain wirings by discharging material comprising conductive nanoparticles and performing a heat treatment of the nanoparticles by a heat lamp or laser. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging method of Jacobson to form the gate and source/drain wiring layer of Ogawa because Jacobson teaches that by using the nanoparticles, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claims 16, 20 and 24, Ogawa discloses that the conductive layer is formed within a semiconductor device that can be incorporated into a display device (col. 21, ln. 60 – col. 22, ln. 5).

Regarding claim 17, Ogawa discloses forming a plurality of gate wirings and gate electrodes (202-204) over a substrate (201), forming an insulating film (207/208) over the gate wirings, laminating a plurality of semiconductor layers (209), a plurality of channel protection layers (219-222), and a plurality of semiconductor layer (214-218/223-230/233-234/239-240) having one of n-type or p-type conductivity over the gate electrode, forming a plurality of pixel electrodes (139/144) arranged in a matrix form over the substrate, and forming a plurality of source wirings (243-247) over the semiconductor layers having the n-type or p-type conductivity such that the source wirings extend across the gate wirings (col. 9, ln. 11 – col. 11, ln. 67). Ogawa discloses that wirings and electrodes are formed by sputtering instead of by discharging conductive material. Like Ogawa, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging method of Jacobson to form the wirings and electrodes of Ogawa because Jacobson teaches that by using the nanoparticles, the problems of harsh and wasteful fabrication conditions can be overcome.

Regarding claim 21, Ogawa discloses forming a plurality of gate wirings and gate electrodes (202-204) over a substrate (201), forming an insulating film (207/208) over the gate wirings, laminating a plurality of semiconductor layers (209), a plurality of channel protection layers (219-222), and a plurality of semiconductor layer (214-218/223-230/233-234/239-240) having one of n-type or p-type conductivity over the gate electrode, forming a plurality of pixel electrodes (139/144) arranged in a matrix form over the substrate, forming a plurality of source wirings (243-247) over the semiconductor layers having the n-type or p-type conductivity such that the source wirings extend across the gate wirings, and forming a second insulating film (249) over the source wirings (col. 9, ln. 11 – col. 11, ln. 67). Ogawa discloses that wirings and electrodes are formed by sputtering instead of by discharging conductive material. Like Ogawa, Jacobson teaches a method of forming a TFT semiconductor device. Jacobson teaches that it is beneficial to form the wirings and the electrodes by discharging material comprising conductive nanoparticles and performing a heat treatment of the nanoparticles by a heat lamp or laser. Each formation of nanoparticles can have its own heat treatment step. Typical semiconductor fabrication processes involve harsh conditions such as high temperatures, caustic chemicals and inefficient subtractive processes. Jacobson teaches that using conductive nanoparticles to form the gate and source/drain layers overcomes all of these problems (col. 1, ln. 32-53; col. 2, ln. 53-67; col. 5, ln. 34 – col. 6, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the conductive nanoparticle discharging method of Jacobson to form the wirings and electrodes of Ogawa because Jacobson teaches that by using the nanoparticles, the problems of harsh and wasteful fabrication conditions can be overcome.

Claims 14, 15, 18, 19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (US 6,362,507) in view of Jacobson et al. (US 6,294,401) as applied to claims 13, 17 and 21 above, and further in view of Speakman (US 6,713,389).

Regarding claims 14, 15, 18, 19, 22 and 23, Ogawa and Jacobson do not disclose the pressure at which the conductive layer is formed. Like Jacobson, Speakman discloses a method of forming conductive wirings of a semiconductor device by depositing droplets of a liquid conductive mixture on the surface of the substrate. Speakman teaches that it is advantageous to form the conductive droplets in a reduced pressure atmosphere because in higher pressures, the droplets will become deformed which impairs its dimensional stability and placement accuracy (col. 40, ln. 10-14). Speakman states that the reduced pressure atmosphere can be in the range of 1×10^5 to 1×10^{-6} N/m^2 (Pa) (col. 4, ln. 6-28).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Hirai et al. (US 6,794,220) disclose a method of printing conductive gate and source/drain wirings of a TFT and annealing the wirings.

Drummond et al. (US 5,132,248) disclose a method of ink-jet printing conductive features on a substrate and laser annealing the features.

Kawase (US 20040253835) discloses a method of ink-jet printing conductive source/drain and gate wirings of a TFT.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
April 13, 2005

Michael Trinh
Primary Examiner